

PATENTS

[your application]

5/5/1 (Item 1 from file: 350)

DIALOG(R)File 350: Derwent WPIX

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0015339140 *Drawing available*

WPI Acc no: 2005-689393/200571

XRPX Acc No: N2005-565881

Encryption key interface system, has universal asynchronous receiver transmitter peripheral for communicating with key variable loader, and driver application for receiving and transmitting commands to key variable loader

Patent Assignee: BOERGER M A (BOER-I)

Inventor: BOERGER M A

Patent Family (1 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050220307	A1	20051006	US 2004814315	A	20040331	200571	B

Priority Applications (no., kind, date): US 2004814315 A 20040331

Patent Details					
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050220307	A1	EN	6	3	

Alerting Abstract US A1

NOVELTY - The system has a **universal asynchronous receiver transmitter (UART)** peripheral (313) for communicating with a **key variable loader (KVL)** through communications link. A driver application is associated with the **UART** peripheral for receiving and transmitting the commands to the **key variable loader**, and a key management application for communication with the driver application for managing the key management information.

DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for using an encryption key interface for communicating key encryption information from a variable key loader (**KVL**) to an electronic device.

USE - Used for transferring encryption keys by utilizing a **universal asynchronous receiver transmitter (UART)** peripheral.

ADVANTAGE - The driver application operates to communicate key command information to **key variable loader** without use of timer peripheral, thus enabling the **key variable loader** to communicate with a broader range of devices utilizing encryption keys without requiring the use of all system processing resources.

DESCRIPTION OF DRAWINGS - The drawing shows a flow chart diagram of the variable key loader connected to a control device using a **UART**.

301 Variable key loader detection

303 **KVL** communication application

305 **UART** peripheral determines

307 **KVL** link layer driver

313 **UART** peripheral

8/5/2 (Item 2 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0018359135 *Drawing available*
WPI Acc no: 2008-M79471/200875
XRPX Acc No: N2008-938335

Precision oscillator for asynchronous transmission system has interface that controls on-chip asynchronous universal receiver transmitter (UART) and provides data interface to UART

Patent Assignee: SILICON LABS CP INC (SILI-N)

Inventor: FERNALD K W; PRIHADI K

Patent Family (1 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20080270817	A1	20081030	US 2002244344	A	20020916	200875	B
			US 2008166229	A	20080701		

Priority Applications (no., kind, date): US 2002244344 A 20020916; US 2008166229 A 20080701

Patent Details						
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20080270817	A1	EN	15	17	Continuation of application	US 2002244344
					Continuation of patent	US 7395447

Alerting Abstract US A1

NOVELTY - An on-chip free running clock circuit generates a temperature compensated clock that provides an on-chip time reference for both a central core processor (140) and an on-chip **UART** (130). An interface between the central core processor and the control and data registers associated with the on-chip **UART** both control the **UART** and provide a data interface to the **UART**.

USE - Precision oscillator for asynchronous transmission system.

ADVANTAGE - Enables communication between on-chip **UART** and off-chip **UART** to be effected **without clock** recovery since off-chip **UART** has independent time reference.

DESCRIPTION OF DRAWINGS - The drawing shows a detailed block diagram of an integrated circuit.

112 Programmable amplifier

130 **UART**

140 Central core processor

150 Internal bus

154 Reset line

8/5/5 (Item 5 from file: 350)
 DIALOG(R)File 350: Derwent WPIX
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0014536087 *Drawing available*
 WPI Acc no: 2004-718039/200470
 XRPX Acc No: N2004-569190

State indicating information setting circuit for use with large scale integrated circuit, has exclusive-OR circuit that receives outputs of first and third D flip-flop circuits and outputs signal to bus driver

Patent Assignee: FUJITSU LTD (FUIT)

Inventor: OKUMURA Y

Patent Family (4 patents, 2 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040193769	A1	20040930	US 2004773232	A	20040209	200470	B
JP 2004295234	A	20041021	JP 200383473	A	20030325	200470	E
US 7159058	B2	20070102	US 2004773232	A	20040209	200703	E
JP 4279023	B2	20090617	JP 200383473	A	20030325	200940	E

Priority Applications (no., kind, date): JP 200383473 A 20030325; US 2004773232 A 20040209

Patent Details						
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20040193769	A1	EN	26	15		
JP 2004295234	A	JA	23			
JP 4279023	B2	JA	23		Previously issued patent	JP 2004295234

Alerting Abstract US A1

NOVELTY - An exclusive-OR circuit receives outputs from the first and second D flip-flop circuits and outputs a status detection signal clearing signal obtained based on exclusive-OR operation of received signals, to an external status detector. An exclusive-OR circuit receives outputs of first and third D flip-flop circuits and outputs a signal obtained based on exclusive-OR operation of received signals, to a bus driver.

DESCRIPTION - An INDEPENDENT CLAIM is also included for status bit setting circuit.

USE - For setting state indicating information of semiconductor circuits such as large scale integrated (LSI) circuit, application specific integrated circuit (ASIC) used in **universal asynchronous receiver-transmitter (UART)** connected to computer.

ADVANTAGE - The state indicating information is set effectively and the state detection signal is cleared rapidly and simultaneously, thus high operation reliability is obtained **without** using any **clock** signal.

DESCRIPTION OF DRAWINGS - **DESCRIPTION OF DRAWING** - The figure shows a circuit diagram of the delta clear to send (DCTS) bit circuit.

10 shot pulse generator

CTS clear to send signal

8/5/9 (Item 9 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0012677634 *Drawing available*

WPI Acc no: 2002-527980/200256

XRPX Acc No: N2002-417982

Network controller for remote devices used in monitoring system, has transmitter transmitting messages with and without clock signals to receiver through common bus, in synchronous and asynchronous modes respectively

Patent Assignee: BOEING CO (BOEI)

Inventor: ELLERBROCK P J; KONZ D W; WINKELMANN J P; ELLERBROCK P; KONZ D;
WINKELMANN J

Patent Family (11 patents, 93 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2002046938	A2	20020613	WO 2001US47393	A	20011109	200256	B
US 20020112070	A1	20020815	US 2000254137	P	20001208	200256	E
			US 2000736878	A	20001214		
AU 200226043	A	20020618	AU 200226043	A	20011109	200262	E
EP 1340153	A2	20030903	EP 2001995467	A	20011109	200365	E
			WO 2001US47393	A	20011109		
JP 2004516698	W	20040603	WO 2001US47393	A	20011109	200436	E
			JP 2002548597	A	20011109		
AU 2002226043	A8	20051006	AU 2002226043	A	20011109	200612	E
EP 1667376	A1	20060607	EP 2001995467	A	20011109	200638	E
			EP 200577656	A	20011109		
US 20060236351	A1	20061019	US 2000254137	P	20001208	200670	E
			US 2000736878	A	20001214		
			US 2006425609	A	20060621		
EP 1892890	A2	20080227	EP 2001995467	A	20011109	200817	E
			EP 200723539	A	20011109		
EP 1340153	B1	20090902	EP 2001995467	A	20011109	200957	E
			WO 2001US47393	A	20011109		
			EP 200577656	A	20051122		
			EP 200723539	A	20071205		
DE 60139803	E	20091015	DE 60139803	A	20011109	200967	E
			EP 2001995467	A	20011109		
			WO 2001US47393	A	20011109		

Priority Applications (no., kind, date): US 2000254137 P 20001208; US 2000736878 A 20001214; US 2006425609 A 20060621

Patent Details					
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes

WO 2002046938	A2	EN	45	6		
National Designated States,Original	AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW					
Regional Designated States,Original	AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW					
US 20020112070	A1	EN			Related to Provisional	US 2000254137
AU 200226043	A	EN			Based on OPI patent	WO 2002046938
EP 1340153	A2	EN			PCT Application	WO 2001US47393
					Based on OPI patent	WO 2002046938
Regional Designated States,Original	AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2004516698	W	JA	79		PCT Application	WO 2001US47393
					Based on OPI patent	WO 2002046938
AU 2002226043	A8	EN			Based on OPI patent	WO 2002046938
EP 1667376	A1	EN			Division of application	EP 2001995467
					Division of patent	EP 1340153
Regional Designated States,Original	AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
US 20060236351	A1	EN			Related to Provisional	US 2000254137
					Division of application	US 2000736878
EP 1892890	A2	EN			Division of application	EP 2001995467
					Division of patent	EP 1340153
Regional Designated States,Original	DE IT					
EP 1340153	B1	EN			PCT Application	WO 2001US47393
					Related to application	EP 200577656
					Related to application	EP 200723539
					Related to patent	EP 1667376
					Related to patent	EP 1892890
					Based on OPI patent	WO 2002046938
Regional Designated States,Original	DE IT					
DE 60139803	E	DE			Application	EP 2001995467
					PCT Application	WO 2001US47393
					Based on OPI patent	EP 1340153
					Based on OPI patent	WO 2002046938

Alerting Abstract WO A2

NOVELTY - A transmitter transmits messages **without clock** signals to a receiver through a common bus (34) at a predetermined bit rate based on received baud select command, in asynchronous mode. The transmitter alternatively transmits both messages and clock signals through the same common bus in synchronous mode.

DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

1. Digital communication method; and
2. Monitoring system.

USE - For digitally controlling remote devices e.g. sensors used in monitoring system (claimed) employed in e.g. avionics industry to monitor strain, acceleration, pressure, corrosion and temperature at various critical structural location of aircraft, in vehicular industry and in multimedia system.

ADVANTAGE - Reduces wiring complexity by connecting the network controller and the remote devices through same common bus. Allows various remote devices to communicate through inexpensive, high speed and robust network line with simple network protocol, small component size and low wire count.

DESCRIPTION OF DRAWINGS - The figure shows a schematic block diagram of an electrical network system implementing network controller.

34 Common bus

8/3,K/10 (Item 10 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0012417278 *Drawing available*
WPI Acc no: 2002-361667/200239
XRPX Acc No: N2002-282702

Comprehensive input/output interface circuit between microprocessor and peripheral device, controls activation/deactivation of operation mode circuits to provide analog/digital input/output function, selectively

Patent Assignee: BOYD L A (BOYD-I); DUTE J C (DUTE-I); DUTEC INC (DUTE-N); ELECTRONIC SOLUTIONS INC (ELSO-N); WOOLWORTH D P (WOOL-I)

Inventor: BOYD L A; DUTE J C; WOOLWORTH D P

Patent Family (6 patents, 94 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2002008867	A2	20020131	WO 2001US23544	A	20010725	200239	B
AU 200184667	A	20020205	AU 200184667	A	20010725	200241	E
US 20020082725	A1	20020627	US 2000220545	P	20000725	200245	E
			US 2001915188	A	20010725		
US 20020083232	A1	20020627	US 2000220545	P	20000725	200245	E
			US 2001916215	A	20010725		
AU 2001284667	A8	20051013	AU 2001284667	A	20010725	200611	E
US 7028105	B2	20060411	US 2000220545	P	20000725	200627	E
			US 2001916215	A	20010725		

Priority Applications (no., kind, date): US 2000220545 P 20000725; US 2001915188 A 20010725; US 2001916215 A 20010725

Patent Details						
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 2002008867	A2	EN	73	27		
National Designated States,Original	AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW					
Regional Designated States,Original	AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW					
AU 200184667	A	EN			Based on OPI patent	WO 2002008867
US 20020082725	A1	EN			Related to Provisional	US 2000220545
US 20020083232	A1	EN			Related to Provisional	US 2000220545
AU 2001284667	A8	EN			Based on OPI patent	WO 2002008867
US 7028105	B2	EN			Related to Provisional	US 2000220545

Alerting Abstract ... data traffic; Electrical input/output interface; Circuit implementing full bidirectional capabilities of normally two-wire **UART** bus serial system; Method for implementing the full bidirectional **capabilities** of multi-wire serial memories over a single microprocessor input/output line; Method for providing... ... basis, independent of any signaling protocol. Controls direction of data transmission over a single conductor **without** a need for **timing** circuits.**Technology Focus** INDUSTRIAL STANDARDS - The interface circuit complies with SPI or **UART** standards. **Extension Abstract** Original Publication Data by AuthorityArgentina**Publication No. ...Original Abstracts:**data flow between a microprocessor (or other device) and a peripheral device having a standard **UART**-based, SPI-based, or similar interface over a **single** input/output (I/O) port line, utilizing the differences of the instantaneous source impedance of... ... signal set for separating the 1-wire data into standard 2-wire and 3-wire **UART**-based, SPI-based, or similar interfaces for use **with** unmodified peripheral devices. The exchange of data on a bit-by-bit or analog basis... ... data flow between a microprocessor (or other device) and a peripheral device having a standard **UART**-based, SPI-based, or similar interface over a single input/output (I/O) **port** line, utilizing the differences of the instantaneous source impedance of the I/O port line... ... signal set for separating the 1-wire data into standard 2-wire and 3-wire **UART**-based, SPI-based, or similar interfaces for use with unmodified peripheral devices. The **exchange** of data on a bit-by-bit or analog basis, with insignificant return delay, allows...

10/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0015023462 *Drawing available*
WPI Acc no: 2005-371439/200538
XRPX Acc No: N2005-300517

Serial port initialization method for use in redundant array of independent disk controller, involves receiving serial port parameter value, for set of selected parameter in order to initialize serial port in controller

Patent Assignee: BALASUBRAMANIAN S (BALA-I); MEREDDY P (MERE-I); LSI CORP (LSIL)
Inventor: BALASUBRAMANIAN S; MEREDDY P

Patent Family (2 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050102433	A1	20050512	US 2003706623	A	20031112	200538	B
US 7415543	B2	20080819	US 2003706623	A	20031112	200857	E

Priority Applications (no., kind, date): US 2003706623 A 20031112; US 2003706623 A 20031112

Patent Details					
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050102433	A1	EN	12	9	

Alerting Abstract ...set of selected serial port parameters including baud rate, number of data and stoop bits, **parity** and flow control. A serial port is initialized in the controller using the received serial... Original Publication Data by AuthorityArgentina**Publication No. ...Original Abstracts:**management window at the host. In addition, an adaptive baud rate negotiation mechanism using the **Universal Asynchronous Receiver Transmitter (UART)** registers in the serial port is provided. The adaptive baud rate negotiation is based on... ... management window at the host. In addition, an adaptive baud rate negotiation mechanism using the **Universal Asynchronous Receiver Transmitter (UART)** registers in the serial port is provided. The adaptive baud rate negotiation is based on... ...**Claims:**and wherein the external device performs the adaptive baud rate negotiation by sending a break **key** sequence from the external device to the storage controller, determining an amount of time between...

14/5/1 (Item 1 from file: 347)
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06692526 **Image available**

AT COMMAND RECEIVING CIRCUIT

Pub. No.: 2000-278356 [JP 2000278356 A]

Published: October 06, 2000 (**20001006**)

Inventor: AOKI YOSHIYUKI

KITAYAMA TOMOHIRO

TSUCHIDA JUNYA

Applicant: NEC CORP

NEC IC MICROCOMPUT SYST LTD

Application No.: 11-082529 [JP 9982529]

Filed: March 25, 1999 (19990325)

International Class: H04L-029/08; H04L-007/04

ABSTRACT

PROBLEM TO BE SOLVED: To provide an AT command receiving circuit capable of measuring a communication speed, identifying the type of a **parity** and a data format to be used for communication and setting this identified information to a universal asynchronous reception/transmission(**UART**) circuit without requiring processing by a CPU at all.

SOLUTION: A speed detecting part 12 and a character receiving part 14 judge the communication speed, the type of the **parity** and the data format from serial data containing respectively received AT commands and this information is written in a **UART** 2 by a communication speed/ **parity** information setting part 16. Besides, a clock supply part 13 generates a clock for data reception and supplies it to the **UART** 2 on the basis of the communication speed detected by the speed detecting part 12.

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14/5/2 (Item 2 from file: 347)
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06113698 **Image available**
SERIAL INTERFACE DEVICE

Pub. No.: 11-055231 [JP 11055231 A]
Published: February 26, 1999 (19990226)
Inventor: SUZUKI TAKASHI
Applicant: MATSUSHITA GRAPHIC COMMUN SYST INC
Application No.: 09-211745 [JP 97211745]
Filed: August 06, 1997 (19970806)
International Class: H04L-007/00; G06F-001/08; G06F-013/00; H04L-007/04

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the throughput of a micro processor by primarily accumulating received data converted in parallel in a shift register or an **UART** part by means of a FIFO system and transferring it to the micro processor.

SOLUTION: A data buffer part 71 is provided between the shift register 61, the **UART** part 1 and the incorporated micro processor 2. Received data which is converted in parallel in the shift register 61 or the **UART** part 1 is primarily stored in the FIFO system and is transferred to the micro processor 2. A status buffer part 71 primarily stores the check result of **parity** and the like by the FIFO system and it is transferred to the micro processor 2. The detection of communication speed which is decided on a user terminal 200-side in one way, the setting of a clock based on the detection and communication speed, the reception and the analysis of an AT command and the format setting of the **UART** part based on the analysis can be realized without depending on the software processing of the incorporated micro processor 2.

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14/5/3 (Item 3 from file: 347)
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03089847 **Image available**

AT COMMAND DETECTING CIRCUIT

Pub. No.: 02-065347 [JP 2065347 A]

Published: March 06, 1990 (**19900306**)

Inventor: KOGYO TAKASHI

Applicant: OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)

Application No.: 63-214798 [JP 88214798]

Filed: August 31, 1988 (19880831)

International Class: [5] H04L-029/06

JAPIO Class: 44.3 (COMMUNICATION -- Telegraphy)

Journal: Section: E, Section No. 931, Vol. 14, No. 241, Pg. 20, May 22, 1990 (19900522)

ABSTRACT

PURPOSE: To add other processing improving input data speed or communication performance by obtaining all information obtained from 'A' or 'a' input data by the external circuit of an MPU when an AT command is detected.

CONSTITUTION: When a DTEC signal is outputted, a speed display bit code decoder and interruption generating circuit 30 output an interruption requesting signal (INT) 54 to an MPU45 and simultaneously, it is decoded which speed of an 'A' and 'a' detecting circuit the DTEC signal is outputted from. The **parity** code of the 'A' or 'a' is added from a **parity** code selector 31 to an above mentioned decode output and inputted to an 'A' and 'a' detected result display register 44. A clock to be suited for the speed is outputted from a UART clock selector 42 and the signal of a next DATA can be received by a UART13.

14/5/4 (Item 4 from file: 347)
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01345942 **Image available**
TERMINAL DEVICE

Pub. No.: 59-057542 [JP 59057542 A]
Published: April 03, 1984 (**19840403**)
Inventor: KAWABATA YOICHI
Applicant: CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
Application No.: 57-167633 [JP 82167633]
Filed: September 28, 1982 (19820928)
International Class: [3] H04L-007/04; H04L-013/00; H04L-025/38
JAPIO Class: 44.3 (COMMUNICATION -- Telegraphy); 45.3 (INFORMATION PROCESSING -- Input Output Units)
Journal: Section: E, Section No. 256, Vol. 08, No. 155, Pg. 78, July 19, 1984 (19840719)

ABSTRACT

PURPOSE: To attain surely the transmission/receiving of data for any user, by changing a Baud rate of transmission/receiving in response to the detection of framing error of a data transmitted from a host computer.

CONSTITUTION: An **universal asynchronous receiver transmitter** UART1 outputs a framing error signal (f) or a **parity** error signal (P), when a framing error or a **parity** error is detected in the information from the host computer. When a control circuit 5 detects the transmission of the signal (f), the circuit 5 controls a selector 4 to select one of plural Baud rate clocks outputted from a frequency division circuit 3 and transmits it to the UART1. The UART1 converts the transmitted data in parallel in the designated Baud rate and transmits it to an input/output control section 6. When the circuit 5 detects the signal P, the circuit 5 controls the UART1, checks the **parity** of the data converted into a parallel data and transmits it to the control section 6.

14/5/5 (Item 5 from file: 347)
DIALOG(R)File 347: JAPIO
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01216044 **Image available**

METHOD FOR TESTING TRANSMISSION LINE

Pub. No.: 58-153444 [JP 58153444 A]

Published: September 12, 1983 (**19830912**)

Inventor: YOKOGAWA HIDEMI
TSUKAMOTO TAKURO
YUMOTO TAKEKO

Applicant: SONY TEKTRONIX CORP [417165] (A Japanese Company or Corporation), JP (Japan)

Application No.: 57-036096 [JP 8236096]

Filed: March 08, 1982 (19820308)

International Class: [3] H04L-013/00; H04L-025/02

JAPIO Class: 44.3 (COMMUNICATION -- Telegraphy); 46.1 (INSTRUMENTATION -- Measurement)

Journal: Section: E, Section No. 214, Vol. 07, No. 272, Pg. 110, December 03, 1983 (19831203)

ABSTRACT

PURPOSE: To measure data transmission line, by displaying an error in addition to an input data and also displaying the positional relation between a search word and a cursor when **parity**, overrun and Fleming errors exist respectively.

CONSTITUTION: When a data fetching start instruction is inputted from a keyboard 54, **USART** (I), (II) convert series data into parallel data, stores data in a data register and also stores the status information of data in a data register at the presence of the information. An address decoder 34 selects the data register and the status register in the **USART** alternately through lines 36, 38, 42, 44. The data and status information in the **USART** is successively stored in the 1st and 2nd areas in an RAM50 of a CPU. When a data display instruction is inputted from the keyboard 54, a cursor address is set up and the data and status to be started from the set up cursor address are displayed on a display device 46 together with the errors of the data and status.

14/5/7 (Item 2 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0016212456 *Drawing available*
WPI Acc no: 2006-744099/200676
Related WPI Acc No: 2008-E19657
XRPX Acc No: N2006-577592

Asynchronous communication link's baud rate detecting method, has adding three remainder bits from shift to baud rate generator during reception and transmission of byte at strategic bit positions

Patent Assignee: ZILOG INC (ZILO-N)

Inventor: NEKI J J; YEARSLEY G D

Patent Family (1 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 7116739	B1	20061003	US 2002284600	A	20021031	200676	B

Priority Applications (no., kind, date): US 2002284600 A 20021031

Patent Details					
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 7116739	B1	EN	6	5	

Alerting Abstract US B1

NOVELTY - The method involves dividing number of clock cycles by number of received bits. The clock cycles are added to a baud rate generator at strategic bit positions during transmission and reception of a data byte based on a remainder value from the dividing step. The reference clock is counted over eight bits and the counter value is divided by eight by shifting three places to the right. The three remainder bits from the shift are added to the generator during the reception and transmission of a byte at strategic bit positions.

USE - Used for detecting a automatic baud rate of an asynchronous communication link, and **UARTs**.

ADVANTAGE - The three remainder bits from the shift are added to the generator during the reception and transmission of the byte at strategic bit positions, thus minimizing framing errors, **parity** errors, and break conditions.

DESCRIPTION OF DRAWINGS - The drawing shows a circuit representation of a baud rate generator.

14/5/12 (Item 7 from file: 350)
 DIALOG(R)File 350: Derwent WPIX
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0014689284 *Drawing available*

WPI Acc no: 2005-036872/**200504**

Related WPI Acc No: 2004-068432

Memory programming method e.g. for electrically erasable programmable read only memory, involves selecting and applying programming voltage to memory based on temperature measured with respect to memory, to program data into memory

Patent Assignee: CYPRESS SEMICONDUCTOR CORP (CYPS)

Inventor: ROUSE M; SNYDER W

Patent Family (1 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6829190	B1	20041207	US 2002172670	A	20020613	200504	B
			US 2003653050	A	20030829		

Priority Applications (no., kind, date): US 2002172670 A 20020613; US 2003653050 A 20030829

Patent Details						
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 6829190	B1	EN	28	10	Continuation of application	US 2002172670
					Continuation of patent	US 6661724

Alerting Abstract US B1

NOVELTY - The method involves assessing a temperature surrounding a memory, using a temperature sensor (230). A programming voltage is selected and applied to the memory for specific time based on the measured temperature, to program data into the memory.

DESCRIPTION - An INDEPENDENT CLAIM is also included for memory programming system.

USE - For programming memory such as flash memory e.g. electrically erasable programmable read only memory (EEPROM) used in digital camera, home video consoles, digital music player, computer. Also for use with functional peripherals such as timers, controllers, serial communication units, cycle **redundancy check (CRC)** generators, **universal asynchronous receiver/transmitter (VART)**, amplifier, voltage pump, programmable gain component, D/A converters, A/D converters, analog drivers, and high/low/band-pass filters.

ADVANTAGE - Selects appropriate programming voltage and time for specific memory, efficiently.

DESCRIPTION OF DRAWINGS - The figure shows a block diagram of the memory programming system.

205 integrated circuit

210 external computing system

220 processor

230 temperature sensor

240 voltage pump

14/5/15 (Item 10 from file: 350)
 DIALOG(R)File 350: Derwent WPIX
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0012949847 *Drawing available*

WPI Acc no: 2003-026709/**200302**

Method for automatically storing mp3 files of narrowband wireless local loop terminal

Patent Assignee: CURITEL COMMUNICATIONS INC (CURI-N); PANTECH&CURITEL CO LTD (PCCO)

Inventor: KIM U B; KIM W B

Patent Family (2 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
KR 2002052769	A	20020704	KR 200082214	A	20001226	200302	B
KR 365732	B	20021227	KR 200082214	A	20001226	200337	E

Priority Applications (no., kind, date): KR 200082214 A 20001226

Patent Details						
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
KR 2002052769	A	KO	1	10		
KR 365732	B	KO			Previously issued patent	KR 2002052769

Alerting Abstract KR A

NOVELTY - A method for automatically storing MP3(MPEG(Moving Picture Experts Group) layer 3) files of an N-WLL(Narrowband-Wireless Local Loop) terminal is provided to allow the N-WLL terminal to automatically capture the MP3 files and store the MP3 files in a memory module, without using an external device such as a **UART(Universal Asynchronous Receiver/Transmitter)** or changing the memory module.

DESCRIPTION - Whether the wireless call processing between a terminal and a base station is a data service is decided(S11). If not, voice call processing is performed(S12), and if a data service, whether a memory pool of the terminal has a margin is decided(S13). If not, data stored in the memory pool are all deleted and the step of S11 is repeated(S14), and if the memory pool has a margin, whether the received data is a frame header of an MP3 file is decided(S15). If not, general data service call processing is performed(S16) and the step of S13 is performed, and if the data correspond to a frame header of an MP3 file, a frame length check and a **CRC(Cyclic Redundancy Check)** are performed(S17). Whether frame length is checked is decided(S18). If not, the step of S16 is performed, and if checked, whether a result value of the **CRC** is coincident with the frame length is decided(S19). If not, the step of S16 is performed, and if coincident, the MP3 file is regarded as correct and stored in a memory module, namely, the memory pool of the terminal(S20).

14/5/18 (Item 13 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0010926635 *Drawing available*

WPI Acc no: 2001-548583/200161

Method for speedily detecting data transmission speed

Patent Assignee: LG ELECTRONICS INC (GLDS); LG INFORMATION & COMMUNICATIONS LTD (GLDS)

Inventor: PARK J Y

Patent Family (2 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
KR 2001028886	A	20010406	KR 199941385	A	19990927	200161	B
KR 386558	B	20030602	KR 199941385	A	19990927	200367	E

Priority Applications (no., kind, date): KR 199941385 A 19990927

Patent Details					
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
KR 2001028886	A	KO	1	10	
KR 386558	B	KO			Previously issued patent KR 2001028886

Alerting Abstract KR A

NOVELTY - A method for speedily detecting a data transmission speed is provided to reduce a length of a stop bit in a data format transmitted to a **UART(Universal Asynchronous Receiver Transmitter)** and to insert information relating to a transmission speed of a next-transmitted data frame to the one part of the stop bit.

DESCRIPTION - If source data(RXDATAS) is inputted to a DEMUX(Demultiplexer)(10), a start bit detector(11) detects start data in an existing inputted data frame. A data bit and a **parity** bit are stored in a shift register(16). A stop bit detector(12) is operated with a clock(UARTCLK) which is faster than a maximum bit speed of a data frame by 16 times. The stop bit detector(12) detects stop bit information during a 9/16 timing. A bit speed information detector(15) detects bit speed information(TXRATEINFO) of a next data frame during a remaining 7/16 timing. The bit speed information detector(15) immediately transmits the bit speed information(TXRATEINFO) to a sampling point detector(14). The bit speed information detector(15) decides a sampling point right from a next data frame start bit detected with the UARTCLK from a timer(13).

14/5/20 (Item 15 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0010533944 *Drawing available*

WPI Acc no: 2001-136354/200114

XRPX Acc No: N2001-099170

Time triggered method in distributed real time computer architecture, involves making time interval between control message and first data message significantly longer than that between successive data messages

Patent Assignee: KOPETZ H (KOPE-I)

Inventor: KOPETZ H

Patent Family (1 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6145008	A	20001107	US 1995527489	A	19950913	200114	B
			US 1997910959	A	19970807		

Priority Applications (no., kind, date): US 1995527489 A 19950913; US 1997910959 A 19970807

Patent Details						
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 6145008	A	EN	10	5	Continuation of application	US 1995527489

Alerting Abstract US A

NOVELTY - A control message has characteristics attribute in one of the value domain and time domain, with even **parity**, while the data message has odd **parity** or vice versa. The time interval between the control message and first data message is significantly longer than time interval between successive data messages.

DESCRIPTION - Every nodes among several nodes has at least one communication channel shared by all nodes with the communication organized into rounds. The structure and attributes of the round are previously defined in a message descriptor list that specifies at which temporal position of the round a node has to send or receive particular message. Every round starts with the control message sent by an active master specifying previously defined message descriptor list that has to be selected for controlling a current round. An **INDEPENDENT CLAIM** is also included for apparatus that implements time triggered method.

USE - For autonomous transmission of messages within distributed real time computer architecture. In automotive industry. Used for non-safety critical real time applications e.g. body electronic applications that use low cost microcontrollers with available communication control units.

ADVANTAGE - Since no hardware modification is necessary, this is a very low cost implementation strategy. Since the physical message format is the same for both implementation strategies, the two implementation strategies can be mixed on single network. Provides autonomously controlled conflict free access to communication channel with predictable temporal properties. Composability in the temporal domain, eliminates all unintended temporal side effects during system integration. Provides short latency for the detection of message errors or node failures. Used on standard serial communication control units (e.g. **UART**, CAN or SAE J1850) that are in widespread use in the industry.

DESCRIPTION OF DRAWINGS - The figure shows the sequence of events during transmission slot in a round.

14/5/21 (Item 16 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0008680323 *Drawing available*

WPI Acc no: 1998-219508/**199820**

XRPX Acc No: N1998-173617

**Protocol for modifying standard Universal Asynchronous Receiver/Transmitter transport -
arranging data in frames of logical grouping of bytes, and first byte of each frame includes start bit
and stop bit, length of message indication and parity bits for entire message or frame**

Patent Assignee: LUCENT TECHNOLOGIES INC (LUCENT)

Inventor: LIU S; LIU S C

Patent Family (9 patents, 26 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 837613	A2	19980422	EP 1997307910	A	19971007	199820	B
CA 2210923	A	19980416	CA 2210923	A	19970721	199835	E
JP 10215496	A	19980811	JP 1997258318	A	19970924	199842	E
KR 1998033036	A	19980725	KR 199754112	A	19971016	199932	E
JP 3681519	B2	20050810	JP 1997258318	A	19970924	200554	E
EP 837613	B1	20060712	EP 1997307910	A	19971007	200652	E
DE 69736314	E	20060824	DE 69736314	A	19971007	200657	E
			EP 1997307910	A	19971007		
KR 476793	B	20050801	KR 199754112	A	19971016	200662	E
DE 69736314	T2	20070705	DE 69736314	A	19971007	200744	E
			EP 1997307910	A	19971007		

Priority Applications (no., kind, date): US 1996732622 A 19961016; EP 1997307910 A 19971007

Patent Details						
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 837613	A2	EN	10	9		
Regional Designated States,Original	AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC NL PT RO SE SI					
CA 2210923	A	EN				
JP 10215496	A	JA	10	9		
KR 1998033036	A	KO		9		
JP 3681519	B2	JA	12		Previously issued patent	JP 10215496
EP 837613	B1	EN				
Regional Designated States,Original	DE FR GB					
DE 69736314	E	DE			Application	EP 1997307910
					Based on OPI patent	EP 837613
KR 476793	B	KO			Previously issued patent	KR 98033036
DE 69736314	T2	DE			Application	EP 1997307910

					Based on OPI patent	EP 837613
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Alerting Abstract EP A2

The messaging protocol for use in a telecommunications network, comprises a message frame containing a number of bytes, each of the bytes including a second number of bits. One of the bytes includes at least one bit defining the number of bytes in the frame, and a number of bits containing **parity** values for the number of bytes. One of the number of bits containing **parity** values is dedicated to one of the number of bytes.

The message frame contains between three and six bytes. Each of the bytes includes eleven bits. Two bits define the number of bytes in the frame. Each of the bytes includes a start bit, a stop bit and a framing bit.

One of the bytes is a header byte defining **parity** values for all of the other of the number of bytes, the **parity** values being defined in a **parity** bit, one **parity** bit being dedicated to each of the other of the number of bytes. The bytes contains control information.

ADVANTAGE - Allows messages of virtually any length.

14/5/25 (Item 20 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0007096387 *Drawing available*

WPI Acc no: 1995-123557/**199516**

XRPX Acc No: N1995-097627

IC card reader-writer control method - using UART as serial transmission circuit and repeating character transmission or command processing when framing or parity errors are detected

Patent Assignee: OKI DENKI KOGYO KK (OKID); OKI ELECTRIC IND CO LTD (OKID)

Inventor: SHONA Y

Patent Family (7 patents, 18 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1995007515	A1	19950316	WO 1994JP1482	A	19940908	199516	B
EP 678828	A1	19951025	EP 1994926370	A	19940908	199547	E
			WO 1994JP1482	A	19940908		
JP 7508585	X	19951005	WO 1994JP1482	A	19940908	199548	E
			JP 1995508585	A	19940908		
US 5790885	A	19980804	WO 1994JP1482	A	19940908	199838	E
			US 1995411808	A	19950410		
KR 275023	B	20001215	WO 1994JP1482	A	19940908	200175	E
			KR 1995701803	A	19950504		
EP 678828	B1	20021127	EP 1994926370	A	19940908	200279	E
			WO 1994JP1482	A	19940908		
DE 69431794	E	20030109	DE 69431794	A	19940908	200312	E
			EP 1994926370	A	19940908		
			WO 1994JP1482	A	19940908		

Priority Applications (no., kind, date): JP 1993225779 A 19930910

Patent Details							
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes		
WO 1995007515	A1	JA	33	10			
National Designated States,Original	JP KR US						
Regional Designated States,Original	AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE						
EP 678828	A1	EN	19	10	PCT Application	WO 1994JP1482	
					Based on OPI patent	WO 1995007515	
Regional Designated States,Original	DE FR GB						
JP 7508585	X	JA	1	1	PCT Application	WO 1994JP1482	
					Based on OPI patent	WO 1995007515	
US 5790885	A	EN			PCT Application	WO 1994JP1482	
					Based on OPI patent	WO 1995007515	
KR 275023	B	KO			PCT Application	WO 1994JP1482	

				Previously issued patent	KR 95704757
				Based on OPI patent	WO 1995007515
EP 678828	B1	EN		PCT Application	WO 1994JP1482
				Based on OPI patent	WO 1995007515
Regional Designated States,Original		DE FR GB			
DE 69431794	E	DE		Application	EP 1994926370
				PCT Application	WO 1994JP1482
				Based on OPI patent	EP 678828
				Based on OPI patent	WO 1995007515

Alerting Abstract WO A1

The control method involves using transmission (TXD) and reception (RXD) lines of a general purpose **UART** circuit (50) directly connected for use as the serial in/out line (L11) of an IC card reader/writer (40). When transmitting, an echo-back character is received for each character transmitted. If the echo is received normally the next character is transmitted while upon detection of a framing error, the previous character is transmitted again.

When receiving, if a **parity** error occurs in the received character the command processing is repeated after completion of command transmission/reception processing.

ADVANTAGE - Simple and economical method of controlling IC card reader/writer using **UART** circuit.

14/5/27 (Item 22 from file: 350)
 DIALOG(R)File 350: Derwent WPIX
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0004531347

WPI Acc no: 1988-280103/198840

Universal async. receiver-transmitter - has parity error and special character recogniser unit on receive side flagging characters placed on FIFO

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)

Inventor: CROWE C; GULICK D E; LAWELL T G

Patent Family (5 patents, 14 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 285334	A	19881005	EP 1988302642	A	19880325	198840	B
JP 63258140	A	19881025	JP 198882135	A	19880401	198848	E
US 4949333	A	19900814	US 198735684	A	19870402	199035	E
			US 1989443088	A	19891127		
EP 285334	B1	19931027	EP 1988302642	A	19880325	199343	E
DE 3885136	G	19931202	DE 3885136	A	19880325	199349	E
			EP 1988302642	A	19880325		

Priority Applications (no., kind, date): US 198735684 A 19870402; US 1989443088 A 19891127

Patent Details							
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes		
EP 285334	A	EN	77	27			
Regional Designated States,Original	AT BE CH DE ES FR GB GR IT LI LU NL SE						
EP 285334	B1	EN	93	27			
Regional Designated States,Original	AT BE CH DE ES FR GB GR IT LI LU NL SE						
DE 3885136	G	DE			Application	EP 1988302642	
					Based on OPI patent	EP 285334	

Alerting Abstract EP A

First-in, first-out registers are provided for both the receiver and transmitter portions, and a **parity** error and special character recogniser unit on the receive side flags characters when they are placed in the receive FIFO. Reception of a special character or one with a **parity** error is reported to the user via an interrupt mechanism. A RAM with the special character recogniser stores user-supplied patterns which are recognised as special characters.

User-accessible status and control registers have bit positions which enable and control the enhanced functions while maintaining compatibility with the industry standard.

ADVANTAGE - Compatible with industry standard yet provides additional features. Can be selectably operated in sync. or async. mode.

14/5/29 (Item 24 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0002706999

WPI Acc no: 1983-742591/198334

Async. digital transmission system for interactive video-text - using arq-nak continuous retransmission with partly check bit on 17 octet code word blocks

Patent Assignee: CENT NAT ETUD TELEC (NATE-N); ETAT FR MIN PTT (ETFR); TELEDIFFUSION DE FRANCE (TELG)

Inventor: BOTREL J; BRIERE J; HARARI S; LOUVEL B

Patent Family (12 patents, 17 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 86128	A	19830817	EP 1983400137	A	19830120	198334	B
FR 2520956	A	19830805	FR 19822120	A	19820204	198336	E
NO 198300357	A	19830829				198341	E
DK 198300431	A	19831010				198347	E
BR 198300634	A	19831108				198401	E
JP 58196744	A	19831116	JP 198316353	A	19830204	198401	E
ES 198401291	A	19840216				198418	E
US 4551839	A	19851105	US 1983460534	A	19830124	198547	E
CA 1223934	A	19870707				198731	E
EP 86128	B	19880518	EP 1983400137	A	19830120	198820	E
DE 3376726	G	19880623				198826	E
SU 1521297	A	19891107	SU 3547558	A	19830203	199022	E

Priority Applications (no., kind, date): FR 19822120 A 19820204

Patent Details					
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
EP 86128	A	FR	42	3	
Regional Designated States,Original		BE CH DE GB IT LI NL SE			
BR 198300634	A	PT			
CA 1223934	A	EN			
EP 86128	B	FR			
Regional Designated States,Original		BE CH DE GB IT LI NL SE			

Alerting Abstract EP A
Data are transmitted in blocks or codewords produced by a code generator and containing 17 bytes for transmission via a parallel-serial converter and a conventional CCITT V23 modem over a switched line of

the public telephone network. The subscriber terminal incorporates a modem, a serial-parallel converter and a codeword receiver.

The first 15 bytes of each codeword comprise characters for transmission and are encoded over 7 bits, the eighth bit being the **parity** check bit. The 16th byte is the codeword control byte, and the 17th is the codeword validation byte which may consist entirely of zeros allowing detection of loss of character synchronisation. The converters and their return-channel counterparts are pref. sections of **universal asynchronous receiver-transmitters**.

18/5/15 (Item 13 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0010782609 *Drawing available*

WPI Acc no: 2001-397620/**200142**

Related WPI Acc No: 2001-335407; 2002-226003

XRPX Acc No: N2001-293061

Message exchanging in secure communication system, involves forming message frame with length field, control field, target destination field, key management message field and CRC field corresponding to message

Patent Assignee: MOTOROLA INC (MOTI)

Inventor: KNAPCZYK S; MURRILL L

Patent Family (6 patents, 22 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2001031837	A1	20010503	WO 2000US23395	A	20000825	200142	B
BR 200014406	A	20020618	BR 200014406	A	20000825	200249	E
			WO 2000US23395	A	20000825		
EP 1226679	A1	20020731	EP 2000959425	A	20000825	200257	E
			WO 2000US23395	A	20000825		
MX 2002003988	A1	20030101	WO 2000US23395	A	20000825	200373	E
			MX 20023988	A	20020422		
MX 231664	B	20051028	WO 2000US23395	A	20000825	200620	E
			MX 20023988	A	20020422		
CA 2387097	C	20080520	CA 2387097	A	20000825	200835	E
			WO 2000US23395	A	20000825		

Priority Applications (no., kind, date): US 1999425816 A 19991022

Patent Details						
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 2001031837	A1	EN	34	6		
National Designated States,Original	BR CA MX					
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
BR 200014406	A	PT			PCT Application	WO 2000US23395
					Based on OPI patent	WO 2001031837
EP 1226679	A1	EN			PCT Application	WO 2000US23395
					Based on OPI patent	WO 2001031837
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
MX 2002003988	A1	ES			PCT Application	WO 2000US23395
					Based on OPI patent	WO 2001031837
MX 231664	B	ES			PCT Application	WO 2000US23395

				Based on OPI patent	WO 2001031837
CA 2387097	C	EN		PCT Application	WO 2000US23395
				Based on OPI patent	WO 2001031837

Alerting Abstract WO A1

NOVELTY - Operation code fields are formed for each message to be exchanged between key delivery device and target communication device. The fields define an operation code indicating the key management message to be exchanged. A message frame with length field, control field, target destination field, key management message field and CRC field is formed, corresponding to the message.

DESCRIPTION - An INDEPENDENT CLAIM is also included for key management message formation method.

USE - In secure communication system such as in-car mobile, hand held portable radio used by police, public safety personnel.

ADVANTAGE - Suitable frame format and message exchange sequence is defined to allow variable length key management messages to be routed through **key variable loader** to the communication device.

Facilitates initiation and termination of exchange of key management message on full duplex and half duplex interfaces.

DESCRIPTION OF DRAWINGS - The figure shows flowchart showing protocol for formation and exchange of messages.

13/3,K/10 (Item 5 from file: 350)
 DIALOG(R)File 350: Derwent WPIX
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0015324393 *Drawing available*
 WPI Acc no: 2005-674642/200569
 XRPX Acc No: N2005-553333

Stand-alone device for use in e.g. remote terminal unit, has microprocessor communicating with computer program script by port connectors, where processor receives/not receives signal, detected by drivers, from device

Patent Assignee: BOGUT D G (BOGU-I); GROSS L C (GROS-I)
 Inventor: BOGUT D G; GROSS L C

Patent Family (1 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050207356	A1	20050922	US 2004803019	A	20040317	200569	B

Priority Applications (no., kind, date): US 2004803019 A 20040317

Patent Details					
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050207356	A1	EN	8	3	

Original Publication Data by AuthorityArgentina**Publication No. ...Original Abstracts:**the serial device to transmit communication parameters to DTE and DCE drivers which communicate via **UART** and pulse width **detectors** with the microprocessor allowing determination and display of communication parameters including Baud Rate and other... **Claims:**DTE Driver and or at least one DCE Driver having outputs to at least one **UART** and or at least one **pulse** width detector; the said at least one DTE Driver and or at least one DCE Driver receiving inputs from the said at least one **UART** and or the said at **least** one pulse width detector; the said at least one **UART** and or the said at **least** one pulse width detector providing outputs to and receiving inputs from the at least one... Driver or the at least one DCE Driver is communicated to the at least one **UART** and the at least one pulse width detector; the output from **the** at least one **UART** and the at least one pulse width detector is communicated by **electronic** means to the at lease one microprocessor; if a signal exists (**270**) then the at... to the lowest value (**280**) and begins the selected script (**290**) for all combinations of **parity** and data bits at the test baud rate based on the user configuration of the script; if the script is successful (**300**) it is an **indication** that the communication parameters were correct for the tested parameters and the results are displayed... is detected then at least one microprocessor displays the current baud rate, data bits, and **parity** and the baud rate, data bits and **parity** are considered correctf. as communication (i.e. an ASCII character prompt) is received from the connected device (**700**) the pulse **width** detector (**100**) reports the widths of each **pulse**; if the minimum pulse width detected is less than half of what is indicated by... Basic Derwent Week: 200569

13/3,K/13 (Item 8 from file: 350)
 DIALOG(R)File 350: Derwent WPIX
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0014689284 *Drawing available*

WPI Acc no: 2005-036872/**200504**

Related WPI Acc No: 2004-068432

Memory programming method e.g. for electrically erasable programmable read only memory, involves selecting and applying programming voltage to memory based on temperature measured with respect to memory, to program data into memory

Patent Assignee: CYPRESS SEMICONDUCTOR CORP (CYPS)

Inventor: ROUSE M; SNYDER W

Patent Family (1 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6829190	B1	20041207	US 2002172670	A	20020613	200504	B
			US 2003653050	A	20030829		

Priority Applications (no., kind, date): US 2002172670 A 20020613; US 2003653050 A 20030829

Patent Details						
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 6829190	B1	EN	28	10	Continuation of application	US 2002172670
					Continuation of patent	US 6661724

Alerting Abstract ...computer. Also for use with functional peripherals such as timers, controllers, serial communication units, cycle **redundancy check (CRC)** generators, **universal asynchronous receiver/transmitter (UART)**, amplifier, voltage pump, programmable gain component, D/A converters, A/D converters, analog drivers ... Basic Derwent Week: **200504**

13/3,K/17 (Item 12 from file: 350)
DIALOG(R)File 350: Derwent WPIX
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0012649041 *Drawing available*

WPI Acc no: 2002-498414/**200253**

High output digital input/output device has primary and secondary data transfer modules having transmit and receive FIFOs selectively adjusted for interact with host computer and digital signal processor

Patent Assignee: 3COM CORP (TCOM)

Inventor: ARNESEN D; KILLIAN H; MESSERLY S

Patent Family (1 patents, 1 countries)							
Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6381661	B1	20020430	US 1999321905	A	19990528	200253	B

Priority Applications (no., kind, date): US 1999321905 A 19990528

Patent Details					
Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 6381661	B1	EN	13	3	

Original Titles:High throughput **UART** to DSP interface having Dual transmit and receive FIFO buffers to support data transfer between... **Alerting Abstract** DESCRIPTION - The primary data transfer module is compatible with standard **universal asynchronous receiver transmitter UART** protocols and timing requirements. The secondary data transfer module is electronically linked to a digital... ... a high output **UART**; and a high output UDIF... ... **ADVANTAGE** - Improves the output of **UART** and DSP interface and relieve the overhead associated with servicing modem interrupts without losing compatibility with standard **UART** protocols, especially when performing data transfer operations. Ensures efficient checking and setting of status flags... ... echo functionality within the hardware interface without excessive DSP involvement. Enables to generate and remove **parity** from data being transmitted through the hardware interface. Allows facing of transfer of data from the **UART** to the DSP by alternatively bursting and halting the data transfers. Enables to emulate data... Original Publication Data by AuthorityArgentina**Publication No. Original Abstracts:**The high throughput **UART** to DSP interface (UDIF) maintains **UART** functionality while integrating dual Transmit (Tx) and Receive (Rx) FIFO buffers that are optimized for... ...DSP overhead required for many of the basic modem functions. The UDIF design also performs **parity** add, **parity** strip, and character echo functions, traditionally performed at a high overhead cost by the DSP**Claims:**high throughput digital Input/Output device comprising: a primary data transfer module compatible with standard **UART** protocols and timing requirements; and a secondary data transfer module electronically linked to a digital... Basic Derwent Week: **200253**

NPL

15/5/1 (Item 1 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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0015620014 **E.I. COMPENDEX No:** 2003377632712

Balanced self-checking asynchronous logic for smart card applications

Moore, Simon; Anderson, Ross; Mullins, Robert; Taylor, George; Fournier, Jacques Jean Alain

Corresp. Author/Affil: Moore, S.: Computer Laboratory, University of Cambridge, Cambridge, United Kingdom

Corresp. Author email: simon.moore@cl.cam.ac.uk

Microprocessors and Microsystems (Microprocessors Microsyst) (Netherlands) 2003 27/9 (421-430)

Publication Date: 20030916

Publisher: Elsevier

CODEN: MIMID **ISSN:** 0141-9331

Publisher Item Identifier: S0141933103000929

Item Identifier (DOI): [10.1016/S0141-9331\(03\)00092-9](https://doi.org/10.1016/S0141-9331(03)00092-9)

Document Type: Conference Paper; Journal **Record Type:** Abstract

Treatment: T; (Theoretical)

Language: English **Summary Language:** English

Number of References: 20

Delay-insensitive or unordered codes may be used to construct both robust asynchronous circuits and self-checking systems. The **redundant** nature of the coding scheme also provides the possibility of a balanced implementation, where the power dissipated is independent of the input data. We demonstrate how these characteristics may be exploited to construct smart card functions that are resistant to both side-channel and fault injection attacks. We also describe how the removal of the clock secures a potential point of attack and enables additional fine-grain timing countermeasures to be introduced. Preliminary results are presented for a smart card test chip containing multiple implementations of a 16-bit micro-controller, a smart card **UART** and a Montgomery modular exponentiator. (c) 2003 Elsevier B.V. All rights reserved.

Descriptors: Encoding (symbols); Formal logic; Microcontrollers; Smart cards; *Microprocessor chips

Identifiers: Asynchronous logic

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits)

721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory))

722.4 (Digital Computers & Systems)

723.2 (Data Processing)

15/5/2 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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0013005706 **E.I. COMPENDEX No:** 1993070996009
Standard data transmission protocols in process control applications

Funk, G.

Corresp. Author/Affil: Funk, G.

European transactions on electrical power engineering (Eur Trans Electr Power Eng) 1992 2/5 (295-302)

Publication Date: 19921201

CODEN: ETEEE **ISSN:** 0939-3072

Document Type: Article; Journal **Record Type:** Abstract

Treatment: A; (Applications); G; (General review); T; (Theoretical)

Language: English **Summary Language:** English

Number of References: 4

The paper describes a standard data transmission protocol that is widely used in telecontrol systems and in field-bus systems for process control applications. The described standard is based on an asynchronous data transmission method that is used for character transmission in office automation systems. The described code guarantees Hamming distance 4 as protection against undetectable message errors. Furthermore, the article describes extensions of the standard code that achieve Hamming distances 6 and 8. The increased data integrity levels of the described data transmission protocols are achieved by defining product codes with single **parity** check codes and BCH codes and by defining special sync characters.

Descriptors: Codes (standards); Control systems; Data communication systems; Local area networks; Process control; Real time systems; Remote control; *Network protocols

Identifiers: Hamming distance 4; Hamming distances 6 and 8; Standard data transmission protocol; Standard frame format FT1.2; Telecontrol systems; **Universal asynchronous receiver transmitter (UART)**

Classification Codes:

722.3 (Data Communication, Equipment & Techniques)

722.4 (Digital Computers & Systems)

723.2 (Data Processing)

731.2 (Control System Applications)

731.3 (Specific Variables Control)

716 (Electronic Equipment, Radar, Radio & Television)

15/5/3 (Item 3 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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0012442366 E.I. COMPENDEX No: 1990110549933

PC communicates with MC. Serial data transfer between PC-AT compatibles and SAB 8051x microcontrollers

Stuerzer, Manfred; Dannhaeuser, Friedrich

Corresp. Author/Affil: Stuerzer, Manfred: Siemens AG, Germany
Siemens components English ed. (Siemens Compon) 1990 25/2 (48-51)

Publication Date: 19900101

CODEN: SICOD **ISSN:** 0173-1734

Document Type: Article; Journal **Record Type:** Abstract

Language: English **Summary Language:** English

In the more complex kind of test and control systems it is often necessary to exchange commands and data between microcontrollers and personal computers. The microcontrollers of the Siemens 8051 family are all fitted with a serial interface, the 80C517 even with two. The settings on the interface and the corresponding settings on the interface device of the AT-compatible PC are described here for transfer rates up to 115.2 kBd.

Descriptors: Computer Interfaces; Computers, Personal; Data Conversion, Analog to Digital; Data Transmission; *Control Equipment

Identifiers: Band Rate; Microcontroller-Computer Data Transfer; **Parity** Bit; PC-MC Data Transfer; Serial Interface; **UART**

15/5/5 (Item 5 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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0010470845 **E.I. COMPENDEX No:** 1976110006994
USART - A UNIVERSAL μ P INTERFACE FOR SERIAL DATA COMMUNICATIONS.

Smith, Lionel

Corresp. Author/Affil: Smith, Lionel

EDN (EDN) 1976 21/16 (81-86)

Publication Date: 19760101

CODEN: EDNSB **ISSN:** 0012-7515

Document Type: Trade Journal **Record Type:** Abstract

Language: Unspecified **Summary Language:** English

A functional description is given of a **USART** (universal synchronous/asynchronous receiver transmitter). In the synchronous mode, the **USART** operates with 5-, 6-, 7- or 8-bit characters. An additional bit can provide even or odd **parity** for error checking. Synchronization can be achieved externally via added hardware, or internally via sync-character detection. To prevent loss of synchronization in the event software fails to supply data in time, single or double sync characters are automatically inserted into the data stream. Asynchronous operation uses the same data and **parity** structures. A **START** and one, one and a half, or two **STOP** bits are appended to this data. The receiver checks proper framing, and a status flag is set if an error occurs. This **USART** can transmit in half- or full-duplex mode and is double-buffered internally (i. e. , the software has a complete character time to respond to a service request).

Descriptors: *DATA TRANSMISSION EQUIPMENT

Classification Codes:

716 (Electronic Equipment, Radar, Radio & Television)

718 (Telephone & Other Line Communications)

15/5/6 (Item 1 from file: 2)
DIALOG(R)File 2: INSPEC
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09167584

Title: USB module for the 16-bit M30624 micro-controller

Author(s): Cebrian, A.; Guill, A.; Millet, J.

Author Affiliation: Dept. de Ingenieria Electron., Univ. Politecnica de Valencia, Spain

Journal: Revista Espanola de Electronica , no.589 , pp.50-5

Publisher: Ediciones Tecnicas Rede

Country of Publication: Spain

Publication Date: Dec. 2003

ISSN: 0482-6396

SICI: 0482-6396(200312)589L:50:MMMC;1-7

CODEN: RVEEBT

Language: Spanish

Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: Implementation of USB peripherals - The recent method of connecting external peripherals to a personal computer was by means of a parallel or serial connection. At the beginning, the parallel port was designed to carry out data transfers from the personal computer to a very specific peripheral, the printer. And the printer is an outgoing peripheral, the flow of data towards it was contemplated, relegating the return to a number of condition indicators (bits). Later, in an attempt to overcome the limitations of the standard parallel port, improvements on the original design were effected, making it bi-directional and increasing the speed of transfer, and the Enhanced Parallel Port made its appearance. On the other hand, the serial port was originally designed for connecting to a bi-directional peripheral, the modem. This inherent, simple to use, bi-directional peripheral converted the serial port into a connection often resorted to in ready-made peripherals that determine exactly an interchange of data with a personal computer. The core of the serial port is the standard **UART (Universal Asynchronous Receiver/ Transmitter)** that has a bi-directional velocity of 115200 bauds, which translates into approximately 10 bi-directional bytes (1 start bit, 8 data bits, 1 parity bit and 1 stop bit for each byte transmitted) (12 refs.)

Subfile(s): B (Electrical & Electronic Engineering); C (Computing & Control Engineering)

Descriptors: electronic data interchange; microcomputers; microcontrollers; modems; peripheral interfaces

Identifiers: USB module; M30624 microcontroller; USB peripherals implementation; personal computer; serial connection; parallel connection; enhanced parallel port; serial port; **UART**; data interchange; **universal asynchronous receiver-transmitter**; universal serial bus module; printer; bidirectional peripheral port; data transfer; modem; USB peripherals; data flow; 16 bit

Classification Codes: B6220J (Modems); B1265F (Microprocessors and microcomputers); C5630 (Networking equipment); C5130 (Microprocessor chips); C5430 (Microcomputers) ; C5610P (Peripheral interfaces); C6130E (Data interchange)

Numerical Indexing: storage capacity: 1.6E+01 bit

INSPEC Update Issue: 2004-044

Copyright: 2004, IEE

15/5/7 (Item 2 from file: 2)
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06873072

Title: Proprietary serial protocols: no help from traditional UARTs

Author(s): Bachiochi, J.

Journal: Circuit Cellar Ink , no.92 , pp.74-8

Publisher: Circuit Cellar Inc

Country of Publication: USA

Publication Date: March 1998

ISSN: 0896-8985

SICI: 0896-8985(199803)92L:74:PSPH;1-O

CODEN: CCINFK

Language: English

Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: On the whole, data accuracy can only be assured by using a well designed protocol. To receive reliable data, start with an accurate transmitter and receiver. Then, add some kind of data check. The most common is the use of **parity** (and it's free with most **UARTs**). In larger packets, like the 64 dataword sized protocol the author needed to design for, you can use checksum or **CRC** data checks built into the packets. It adds a bit of overhead to the receive routines to ensure accurate reception and also requires a method of requesting retransmission of a damaged data packet from the transmitter. So, the next time you have a communication job to do, make use of that good old standard, the hardware **UART**. But if the bits get out of control, take over and bang them into submission. Just remember to get out your slide rule and check the system tolerances (0 refs.)

Subfile(s): C (Computing & Control Engineering)

Descriptors: computer interfaces; data communication equipment; data integrity; packet switching; protocols

Identifiers: traditional **UARTs**; data accuracy; proprietary serial protocols; reliable data; accurate transmitter; receiver; data check; **parity**; 64 dataword sized protocol; checksum; **CRC** data checks; requesting retransmission; damaged data packet; communication job; hardware **UART**

Classification Codes: C5690 (Other data communication equipment and techniques); C5610 (Computer interfaces); C5640 (Protocols); C6130 (Data handling techniques)

INSPEC Update Issue: 1998-013

Copyright: 1998, IEE

15/5/9 (Item 4 from file: 2)
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03879725

Title: Multivision for amateurs and professionals: fade- and change-over control for four dia-projectors. I

Author(s): Hohlein, H.

Journal: Funkschau , no.1 , pp.60-6

Country of Publication: West Germany

Publication Date: 2 Jan. 1987

ISSN: 0016-2841

CODEN: FUSHA2

Language: German

Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: A DIY genuine multivision mixer is described, capable of independent processing of 4 analog and/or digital channels. The core of the equipment is the **UART (Universal Asynchronous Receiver-Transmitter)**, contained in the IM 6402 chip, which consists of paired buffers, registers, **parity**- and start/stop circuits and multiplexers for receive and send modes; it is described with the aid of a separate block diagram. The rest of the equipment, using 17 ICs, includes a 2 MHz clock generator, A/D converter, multiplexers feeding the **UART** and demultiplexers leaving it, FSK modems for record and replay and 4 channel drivers. Illustrations include 2 circuit diagrams (board of equipment and control console), 2 block diagrams, pulse waveforms, components list, 4 printed board drawings and 2 photographs (5 refs.)

Subfile(s): B (Electrical & Electronic Engineering)

Descriptors: television equipment

Identifiers: TV equipment; multivision mixer; **UART**; IM 6402; demultiplexers; FSK modems

Classification Codes: B6430 (Television equipment, systems and applications)

INSPEC Update Issue: 1987-012

Copyright: 1987, IEE

15/5/10 (Item 5 from file: 2)
DIALOG(R)File 2: INSPEC
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03706487

Title: Reduce noise in a serial bit stream

Author(s): Strom, S.

Author Affiliation: Nat. Semicond., Mesa, AZ, USA

Journal: EDN , vol.31 , no.9 , pp.266

Country of Publication: USA

Publication Date: 1 May 1986

ISSN: 0012-7515

CODEN: EDNSBH

Language: English

Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: As an FSK receiver's input signal shifts between two frequencies, the receiver's output switches between two logic levels, producing a serial stream of pulses. The pulse stream normally goes to a **UART** or similar device, which samples the data once in the middle of each bit interval; however, a noisy input signal can create spurious output pulses that appear as invalid data to the **UART**. It is possible to detect faulty data using **parity** or **CRC** (cyclic **redundancy checking**) techniques, but the system must then retransmit the data packet, slowing the throughput. To preserve a high throughput rate, data errors should be removed before they reach the **UART** (0 refs.)

Subfile(s): B (Electrical & Electronic Engineering)

Descriptors: frequency shift keying; interference suppression; pulse circuits

Identifiers: serial bit stream; FSK; logic levels; pulse stream; **UART**; bit interval; noisy input signal; faulty data; **parity**; **CRC**; cyclic **redundancy checking**; data packet

Classification Codes: B1260 (Pulse circuits); B6120 (Modulation and coding methods); B6200 (Telecommunication)

INSPEC Update Issue: 1986-016

Copyright: 1986, IEE

15/5/12 (Item 7 from file: 2)
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03374884

Title: Serial data communications: always in turn

Author(s): Plate, J.

Journal: Funkschau , no.20 , pp.70-1

Country of Publication: West Germany

Publication Date: 28 Sept. 1984

ISSN: 0016-2841

CODEN: FUSHA2

Language: German

Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: Parallel/series transforms are needed whenever bytes have to be transmitted by telephone. Conversion is done by shift registers, ambiguities are avoided by framing procedures, requiring start- and stop bits. Asynchronous transmission modes are then briefly explained, improved by **parity** bits and by the use of 'intelligent' UARTs (**Universal Asynchronous Receiver/Transmitter**) with individual control codes, initiated by a OPEN command. The more universal hardware protocol method ensures secure data flows to peripherals like printers; it is briefly described. Three simple diagrams, and a view of the generally used RS-232-C plug are included (0 refs.)

Subfile(s): B (Electrical & Electronic Engineering); C (Computing & Control Engineering)

Descriptors: data communication systems

Identifiers: asynchronous transmission; data communications; telephone; shift registers; framing;

UARTs; control codes; OPEN command; hardware protocol; secure data flows; RS-232-C plug

Classification Codes: C5610N (Network interfaces); C5610P (Peripheral interfaces); B6210Z (Other data transmission)

INSPEC Update Issue: 1985-004

Copyright: 1985, IEE

15/5/13 (Item 8 from file: 2)
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03272363

Title: Ubiquitous UART speeds digital-RF interfacing

Author(s): Sproul, R.

Author Affiliation: Lorch Electronics, Englewood, NJ, USA

Journal: Microwaves & RF , vol.23 , no.1 , pp.113, 115

Country of Publication: USA

Publication Date: Jan. 1984

ISSN: 0745-2993

CODEN: MIRFDL

Language: English

Document Type: Journal Paper (JP)

Treatment: General or Review (G)

Abstract: The author provides a brief but comprehensive review of the **universal asynchronous receiver/transmitter (UART)**, a cheap, yet relatively sophisticated parallel-to-serial interface. The operation of the device is explained and the **parity** principle illustrated. Inexpensive **UARTs** operate at rates of a few thousand bits per second, while slightly costlier units can achieve rates of several hundred thousand bits per second with rates of hundreds of megabits per second possible. All **UARTs** have the same physical characteristics and have identical types of interconnections, regardless of price or level of performance. A block diagram shows the complexity of the device which can be fitted into a standard 40 pin package. The author then considers the **UART** characteristics and performance, with a final brief mention of standardisation in data transmission (*0 refs.*)

Subfile(s): B (Electrical & Electronic Engineering); C (Computing & Control Engineering)

Descriptors: computer interfaces; data communication equipment; digital integrated circuits

Identifiers: data communication equipment; computer interfaces; digital IC; **UART**; digital-RF interfacing; **universal asynchronous receiver/transmitter**; parallel-to-serial interface

Classification Codes: B1265Z (Other digital circuits); C5610 (Computer interfaces)

INSPEC Update Issue: 1984-008

Copyright: 1984, IEE

15/5/15 (Item 10 from file: 2)
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02833377

Title: Using UARTS. I

Author(s): Burchell, J.C.

Journal: Radio & Electronics World , pp.56-7

Country of Publication: UK

Publication Date: Dec. 1981

ISSN: 0262-2572

CODEN: RELWDZ

Language: English

Document Type: Journal Paper (JP)

Treatment: Application (A); Practical (P)

Abstract: The **universal asynchronous receiver/ transmitter (UART)** provides an extremely effective interface between a computer's serial in/out port and a parallel real world. Nearly all home/personal computers are equipped with a serial RS232 port. By using a **UART** to communicate with this port it becomes possible to use it for an extensive variety of interface tasks. To use a **UART** successfully three criteria must be satisfied. Firstly, the device must be electrically interfaced to the RS232 signal levels in the computer's interface port. Secondly, the **UART** must be supplied with a precise clock frequency to synchronise and time the transmission and reception of all data. Thirdly, the parameters of the data stream i.e. number of data bits, **parity** bit selection, number of stop bits, must be established at both ends of the communication link (0 refs.)

Subfile(s): B (Electrical & Electronic Engineering); C (Computing & Control Engineering)

Descriptors: computer interfaces; data communication equipment; digital integrated circuits

Identifiers: **universal asynchronous receiver/ transmitter**; serial RS232 port; RS232 signal levels; precise clock frequency; data stream; **parity** bit selection

Classification Codes: B1265Z (Other digital circuits); C5610 (Computer interfaces)

INSPEC Update Issue: 1982-004

Copyright: 1982, IEE

15/5/16 (Item 11 from file: 2)
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02684695

Title: Input/output device connection to the 'PDV' digital electronic process control bus

Author(s): Dillmann, R.; Rotert, M.

Author Affiliation: Inst. for Informatik III, Tech. Univ. Karlsruhe, Karlsruhe, West Germany

Journal: Elektronik , vol.30 , no.5 , pp.93-101

Country of Publication: West Germany

Publication Date: 13 March 1981

ISSN: 0013-5658

CODEN: EKRKAR

Language: German

Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: The V24 and DIN6602 interfaces are compared in detail, possible network interconnections are illustrated and reference is made to cyclic **redundancy checks**. The use of software controlled **UART** and **ACIA** (asynchronous communications interface) devices is also discussed and flow diagrams are presented, with special reference to the type M6800 microprocessor. Comparisons are made with the IEEE bus, the CAMAC system and the DEC 'Dataway' (8 refs.)

Subfile(s): C (Computing & Control Engineering)

Descriptors: computer interfaces

Identifiers: process control bus; V24; DIN6602; interfaces; network interconnections; cyclic **redundancy checks**; **UART**; **ACIA** ; M6800; IEEE bus; CAMAC system; Dataway

Classification Codes: C5610 (Computer interfaces)

INSPEC Update Issue: 1981-006

Copyright: 1981, IEE

15/5/22 (Item 17 from file: 2)
DIALOG(R)File 2: INSPEC
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02006474

Title: Microcomputer interfacing: a software UART

Author(s): Field, P.E.; Rony, P.R.; Larsen, D.G.; Titus, J.A.

Author Affiliation: Virginia Polytech. Inst. & State Univ., Blacksburg, VA, USA

Journal: Computer Design , vol.15 , no.10 , pp.118-20

Country of Publication: USA

Publication Date: Oct. 1976

ISSN: 0010-4566

CODEN: CMPDAM

Language: English

Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: The hardware device discussed is the **universal asynchronous receiver/transmitter**, a 40-pin integrated circuit chip that contains an independent 8-bit asynchronous receiver and independent 8-bit asynchronous transmitter. Data rates range from DC to 60K bits/s. Receiver and transmitter sections of the chip can be programmed for five, six, seven, or eight data bits, one or two stop bits, even or odd **parity**, and **parity** or no **parity**. The chip also contains a variety of flags (6 refs.)

Subfile(s): C (Computing & Control Engineering)

Descriptors: computer interfaces; microcomputers

Identifiers: software; **universal asynchronous receiver/ transmitter**; integrated circuit chip; flags; microcomputer interfacing

Classification Codes: C5610 (Computer interfaces)

INSPEC Update Issue: 1977-002

Copyright: 1977, IEE

15/5/23 (Item 18 from file: 2)
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01806146

Title: Detecting transmission errors

Author(s): Watson, N.R.; Shenton, G.D.

Journal: Systems International , vol.3 , no.3 , pp.23-4

Country of Publication: UK

Publication Date: April 1975

ISSN: 0309-1171

CODEN: SYIND8

Language: English

Document Type: Journal Paper (JP)

Treatment: Application (A); Practical (P); Theoretical or Mathematical (T)

Abstract: Describes the AMI S9544 CRC encoder/decoder for error detection in data transmission systems. Parallel data is converted to serial data and reconverted to parallel at the receiver by a **universal asynchronous receiver transmitter**, e.g. the AMI S1757. Errors are detected by means of a cyclic **redundancy check**-the encoder is placed in the serial data stream at the transmitter and the decoder at the receiver (3 refs.)

Subfile(s): B (Electrical & Electronic Engineering); C (Computing & Control Engineering)

Descriptors: data transmission systems; digital communication systems; encoding; error detection; fault tolerant computing

Identifiers: AMI S9544 CRC encoder/decoder; error detection; data transmission systems; **universal asynchronous receiver transmitter**; cyclic **redundancy check**; parallel/serial conversion; serial/parallel conversion; transmission error detection

Classification Codes: B6120B (Codes); C5600 (Data communication equipment and techniques)

INSPEC Update Issue: 1975-008

Copyright: 1975, IEE

15/5/35 (Item 1 from file: 23)
DIALOG(R)File 23: CSA Technology Research Database
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0010405210 IP Accession No: 200809-71-1712337; 200809-61-1814588; 20081665154; A08-99-1768823

Enhanced universal asynchronous receiver-transmitter

Gulick, Dale E; Lawell, Terry G; Crowe, Charles
, USA

Publisher Url: <http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=4949333.PN.&OS=pn/4949333&RS=PN/4949333>

Document Type: Patent

Record Type: Abstract

Language: English

File Segment: Metadex; Mechanical & Transportation Engineering Abstracts; ANTE: Abstracts in New Technologies and Engineering; Aerospace & High Technology

Abstract:

A **universal asynchronous receiver-transmitter (UART)** (54) is disclosed which is compatible with an industry standard yet provides additional features. The **UART** can be selectably operated in a synchronous or an asynchronous mode. First-in, first-out (FIFO) registers (404,424) are provided for both the receiver and transmitter portions of the **UART**, and a **parity** error and special character recognizer unit (412) on the receive side flags characters when they are placed in the receive FIFO. Reception of a special character or one with a **parity** error is reported to the user via an interrupt mechanism (430). A random access memory (RAM) (413) with the special character recognized stores user-supplied patterns which are recognized as special characters. User-accessible status and control registers (408) have bit positions which enable and control the enhanced functions of the **UART** while maintaining compatibility with the industry standard.

Descriptors: **UART**; Registers; Random access memory; Industry standards; **Parity**; Errors; Interrupts; Synchronous; Receivers; Compatibility; Transmitters; Flags

Subj Catg: 71, General and Nonclassified; 61, Design Principles; 99, General